regions to be silicided;

depositing a titanium layer directly overlying said silicon regions to be silicided;

subjecting said substrate to a first annealing whereby said titanium is transformed to phase C40 titanium disilicide where it overlies said silicon regions and wherein said titanium not overlying said silicon regions is unreacted;

subjecting said substrate to a second annealing at a temperature of less than 700 ^{o}C whereby said phase C40 titanium disilicide is transformed to phase C54 titanium disilicide; and

removing said unreacted titanium disilicide to complete formation of said titanium disilicide film in the manufacture of said integrated circuit.

REMARKS

Examiner J. Maldonado is thanked for the thorough examination and search of the subject Patent Application. Claims 1, 8, and 15 have been amended.

The Specification has been amended to include the wavelength "of 248 nm and energy of" inadvertently left out of the sentence. This wavelength of 248 is claimed in Claims

5, 12, and 19.

All Claims are believed to be in condition for Allowance and that is so requested.

Reconsideration of the rejection of Claims 1, 8, and 15 under 35 U.S.C. 112, first paragraph is requested in accordance with the following remarks.

The Examiner says that the disclosure of Applicants' invention is not enabling because it does not disclose the presence of refractory metals in forming $TiSi_2$ as taught in the paper to Mouroux cited by the Examiner. Applicants respectfully submit that while the method of Mouroux may be one way to form C54 $TiSi_2$, this method is not used and is not required by Applicants' invention. On page 6 of the Specification, Applicants noted that there may be other ways than their invention of forming C40 $TiSi_2$ such as by RTA. Mouroux's method may be one of these other ways. However, Applicants' method of forming C40 $TiSi_2$ by laser annealing has been proved by experimentation. Thus, it is not agreed that the presence of refractory metals is required to form C40 $TiSi_2$.

Reconsideration of the rejection of Claims 1, 8, and 15 under 35 U.S.C. 112, first paragraph is requested in accordance with the following remarks.

Reconsideration of the rejection under 35 U.S.C. 102 of Claims 1, 2, 6, 7, 15, 16, 20, and 21 as being anticipated by Mouroux is requested in view of Amended Claims 1 and 15 and in accordance with the following remarks.

It is agreed that Mouroux teaches a method of forming C40 and then C54 titanium silicide. However, Mouroux requires the presence of a refractory metal layer such as Mo underlying the Ti layer to form the C40 phase. Applicants' do not use a refractory metal layer in forming the C40 phase TiSi2. It is the laser annealing that forms the C40 phase in Applicants' invention. Claims 1 and 15 have been amended to state that the titanium layer is deposited directly overlying the silicon regions to be silicided as shown in the figures. This clearly differentiates the claims over Mouroux since Mouroux requires an intervening layer of Nb or Mo (see for example page 25).

Reconsideration of the rejection under 35 U.S.C. 102 of Claims 1, 2, 6, 7, 15, 16, 20, and 21 as being anticipated by Mouroux is requested in view of Amended Claims 1 and 15 and

in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 3 and 7 as being unpatentable over Mouroux is requested in view of Amended Claim 1 and in accordance with the following remarks.

Claim 1 has been amended to state that the titanium layer is deposited directly overlying the silicon regions to be silicided as shown in the figures. This clearly is different from Mouroux since Mouroux requires an intervening layer of Nb or Mo to form the C40 phase $TiSi_2$.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 3 and 7 as being unpatentable over Mouroux is requested in view of Amended Claim 1 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 4, 5, 8-14, 18, and 19 as being unpatentable over Mouroux in view of Ishida is requested in view of Amended Claims 1, 8, and 15 and in accordance with the following remarks.

Claims 1, 8, and 15 have been amended to state that the titanium layer is deposited directly overlying the silicon regions to be silicided as shown in the figures. This clearly is different from Mouroux since Mouroux requires an intervening layer of Nb or Mo to form the C40 phase $TiSi_2$. Ishida was cited in the background section of the Specification. On page 6, it is stated that Applicants' process is a solid state process wherein the energy is adjusted carefully so as not to melt the silicon. In contrast, Ishida melts the silicon (see col. 4, lines 27-30). Thus, it is not agreed that the process parameters of the laser annealing step are obvious since Applicants require that melting the silicon be avoided while Ishida desires melting of the silicon.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 4, 5, 8-14, 18, and 19 as being unpatentable over Mouroux in view of Ishida is requested in view of Amended Claims 1, 8, and 15 and in accordance with the remarks above.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES

MADE."

It is requested that should Examiner Maldonado not find that the Claims are now Allowable that he call the undersigned at 765 4530866 to overcome any problems preventing allowance.

Respectfully submitted,

Rosemary L. S. Pike. Reg # 39,332

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please amend the paragrpah bridging pages 6 and 7 as follows:

Now, the wafer is subjected to a laser annealing process 30. A Nd:YAG laser may be used, having a wavelength of 1.06 nm and energy of between about 0.5 and 1.5 Joules/cm^2. Preferably, a KrF Excimer laser is used, having a wavelenghth of 248 nm and energy of between about 0.1 and 1.2 Joules/cm^2. A prior art approach uses very high laser energy to melt the silicon. In the process of the present invention, a solid state reaction process is used. The laser energy must be adjusted carefully so as not to cause melting of the silicon. It is possible that C40 titanium disilicide could be formed by another process, such as RTA. However, the laser annealing process of the present invention has been proved experimentally. This annealing will form phase C40 titanium disilicide ($TiSi_2$) 32 over the gate electrode and over the source and drain regions, as shown in Fig. 3. C40 titanium disilicide has a crystal lattice structure very similar to that of C54, but quite different from that of C49. The extreme non-equilibrium of the laser annealing process of the invention favors the formation of meta-stable phase C40

$TiSi_2$.

IN THE CLAIMS

Please amend the Claims as follows:

1. (AMENDED) A method of fabricating a titanium disilicide film in the manufacture of an integrated circuit comprising:

providing a semiconductor substrate having silicon regions to be silicided;

depositing a titanium layer directly overlying said silicon regions to be silicided;

subjecting said substrate to a first annealing whereby said titanium is transformed to phase C40 titanium disilicide where it overlies said silicon regions and wherein said titanium not overlying said silicon regions is unreacted;

subjecting said substrate to a second annealing whereby phase C54 titanium disilicide is grown overlying said phase C40 titanium disilicide and whereby said phase C40 titanium disilicide is transformed to phase C54 titanium disilicide; and

removing said unreacted titanium layer to complete formation of said titanium disilicide film in the

manufacture of said integrated circuit.

8. (AMENDED) A method of fabricating a titanium disilicide film in the manufacture of an integrated circuit comprising:

providing a semiconductor substrate having silicon regions to be silicided;

depositing a titanium layer directly overlying said silicon regions to be silicided;

subjecting said substrate to a laser annealing whereby said titanium is transformed to phase C40 titanium disilicide where it overlies said silicon regions and wherein said titanium not overlying said silicon regions is unreacted;

subjecting said substrate to a low temperature annealing whereby said phase C40 titanium disilicide is grown overlying said phase C40 titanium disilicide and whereby said phase C40 titanium disilicide is transformed to phase C54 titanium disilicide; and

removing said unreacted titanium layer to complete formation of said titanium disilicide film in the manufacture of said integrated circuit.

15. (AMENDED) A method of fabricating a titanium disilicide film in the manufacture of an integrated

circuit comprising:

providing a semiconductor substrate having silicon regions to be silicided;

depositing a titanium layer directly overlying said silicon regions to be silicided;

subjecting said substrate to a first annealing whereby said titanium is transformed to phase C40 titanium disilicide where it overlies said silicon regions and wherein said titanium not overlying said silicon regions is unreacted;

subjecting said substrate to a second annealing at a temperature of less than 700 ^{o}C whereby said phase C40 titanium disilicide is transformed to phase C54 titanium disilicide; and

removing said unreacted titanium disilicide to complete formation of said titanium disilicide film in the manufacture of said integrated circuit.